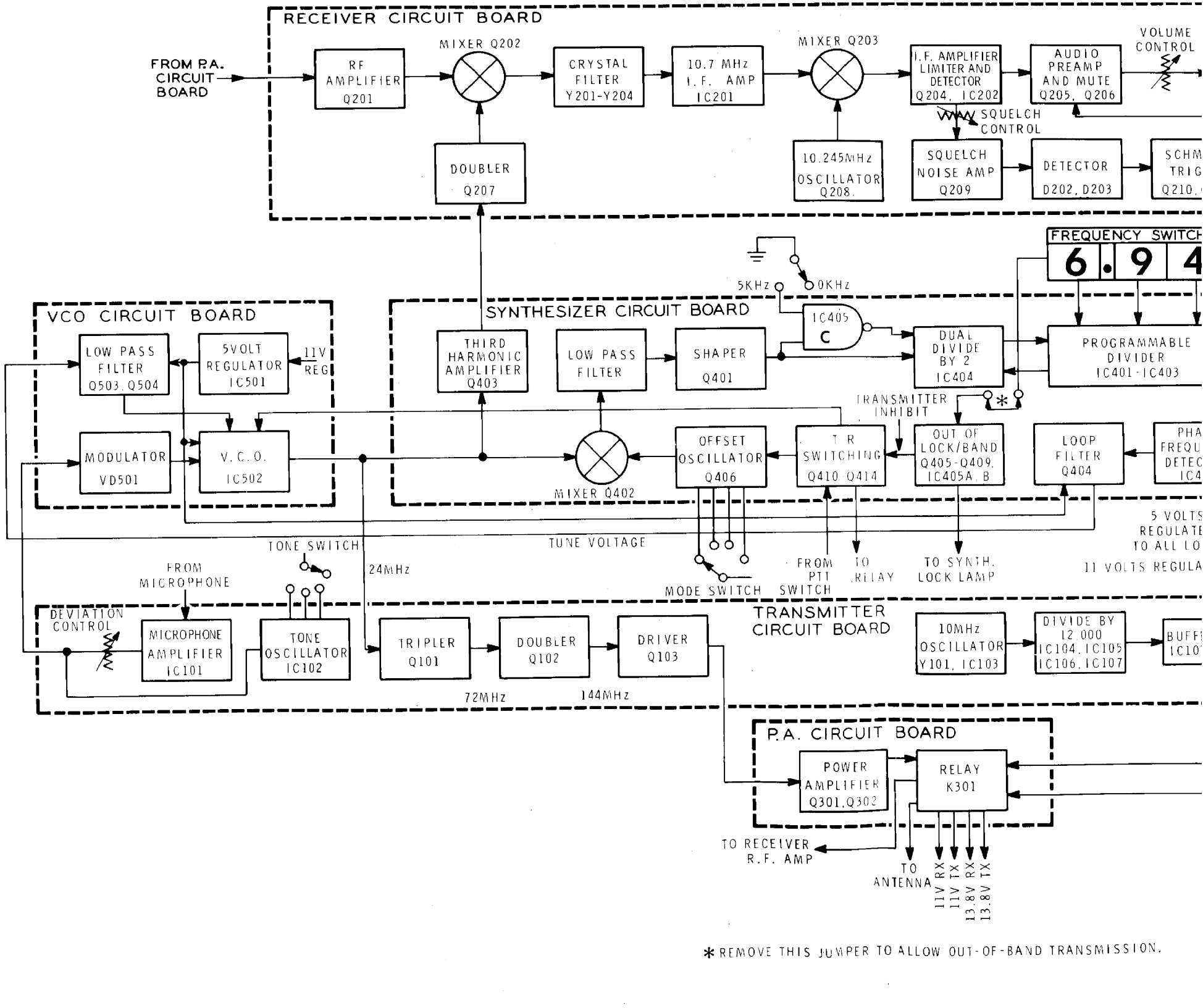
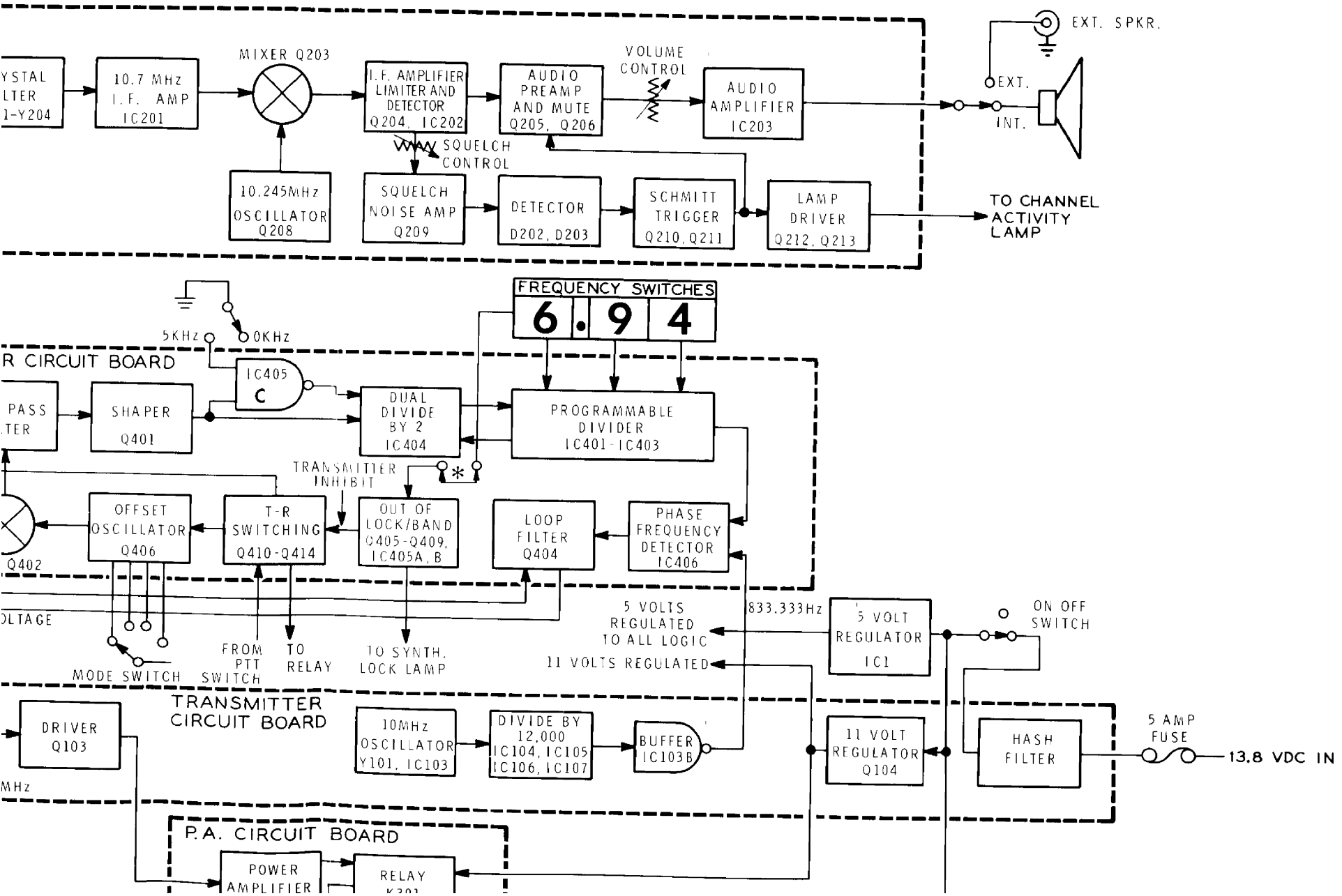

RECEIVER CIRCUIT BOARD
FROM P.A. CIRCUIT BOARD
RF AMPLIFIER Q201
MIXER Q202
CRYSTAL FILTER Y201-Y204
10.7 MHz I.F. AMP IC201
MIXER Q203
I.F. AMPLIFIER LIMITER AND DETECTOR Q204, IC202
AUDIO PREAMP AND MUTE Q205, Q206
VOLUME CONTROL
SQUELCH CONTROL
DOUBLER Q207
10.245MHz OSCILLATOR Q208
SQUELCH NOISE AMP Q209
DETECTOR D202, D203
SCHM TRIG Q210,
FREQUENCY SWITCH
6.9 4
5KHz
0KHz
VCO CIRCUIT BOARD
LOW PASS FILTER Q503, Q504
5VOLT REGULATOR IC501
11V REG
MODULATOR VD501
V.C.O. IC502
SYNTHESIZER CIRCUIT BOARD
THIRD HARMONIC AMPLIFIER Q403
LOW PASS FILTER
SHAPER Q401
IC405 C
DUAL DIVIDE BY 2 IC404
PROGRAMMABLE DIVIDER IC401-IC403
TRANSMITTER INHIBIT
MIXER Q402
OFFSET OSCILLATOR Q406
T R SWITCHING Q410 Q414
OUT OF LOCK/BAND Q405-Q409, IC405A, B
LOOP FILTER Q404
PHA FREQU DETEC IC4
5 VOLTS REGULATE TO ALL LO
11 VOLTS REGULA
TONE SWITCH
TUNE VOLTAGE
FROM MICROPHONE
24MHz
MODE SWITCH
FROM PTT SWITCH
TO RELAY
TO SYNTH. LOCK LAMP
DEVIATION CONTROL
MICROPHONE AMPLIFIER IC101
TONE OSCILLATOR IC102
TRIPLER Q101
DOUBLER Q102
DRIVER Q103
TRANSMITTER CIRCUIT BOARD
10MHz OSCILLATOR Y101, IC103
DIVIDE BY 12,000 IC104, IC105 IC106, IC107
BUFF IC10
72MHz
144MHz
P.A. CIRCUIT BOARD
POWER AMPLIFIER Q301, Q302
RELAY K301
TO RECEIVER R.F. AMP
TO ANTENNA
11V RX
11V TX
13.8V RX
13.8V TX
* REMOVE THIS JUMPER TO ALLOW OUT-OF-BAND TRANSMISSION.

Untitled

BLOCK DIAGRAM



SYNTHESIZER

GENERAL

The synthesizer circuit board receives an 833.333 Hz reference signal from the transmitter circuit board and also the output signal from the voltage-controlled oscillator (VCO) on the VCO circuit board. The frequency of the signal coming from the VCO circuit board is one-sixth the desired transmitter frequency in the transmit modes, and is automatically switched in the receive mode so that, when multiplied by six, it provides a receiver injection signal that is 10.7 MHz below the receive frequency selected on the front panel switches.

The accuracy and stability of the VCO are proportional to the combined accuracy and stability of two temperature-compensated, crystal-controlled oscillators. One of these oscillators operates at 10 MHz and provides the 833.333 Hz reference signal. The other oscillator (offset oscillator) operates in the 20 MHz range. The VCO is phase-locked to these two oscillators. If the VCO becomes unlocked, the red "Synth Lock" LED will light. If this unlocked condition lasts for more than about one-half second, the transmitter is automatically disabled to prevent operation outside the band. This inhibit circuitry also disables the transmitter if the front panel switches are set below 144.000 MHz or above 147.995 MHz. This feature can be defeated if you desire to operate on MARS or CAP frequencies.

Transistor Q402 mixes the output of the offset oscillator (Q406) with the output of the VCO. A low-pass filter, consisting of C404 and L401 passes the difference signal to Q401 where it is shaped to be compatible to drive a programmable divider formed by IC401 through IC404. When the VCO is on the frequency that corresponds to that selected on the front panel switches, the output of the programmable divider is 833.333 Hz. If the VCO is not on the correct frequency, the output of the programmable divider is other than 833.333 Hz, which is required for lock.

IC406 compares the output frequency of the programmable divider to the 833.333 Hz reference. If they are equal, the tune voltage to the VCO remains unchanged and IC406 phase-locks the loop. If they are not equal, the phase-frequency detector, IC406, puts out pulses which are integrated (averaged) by loop filter Q404. This changes the tune voltage in the proper direction to tune the VCO toward the correct frequency and brings the output of the programmable divider toward 833.333 Hz (establishing the locked condition).

PROGRAMMABLE DIVIDER

The programmable divider, (see Figure 1) consists of IC401, IC402, IC403, and IC404. IC401, IC402, and IC403 are cascaded programmable, decade down-counters. The divisor, which is the number selected

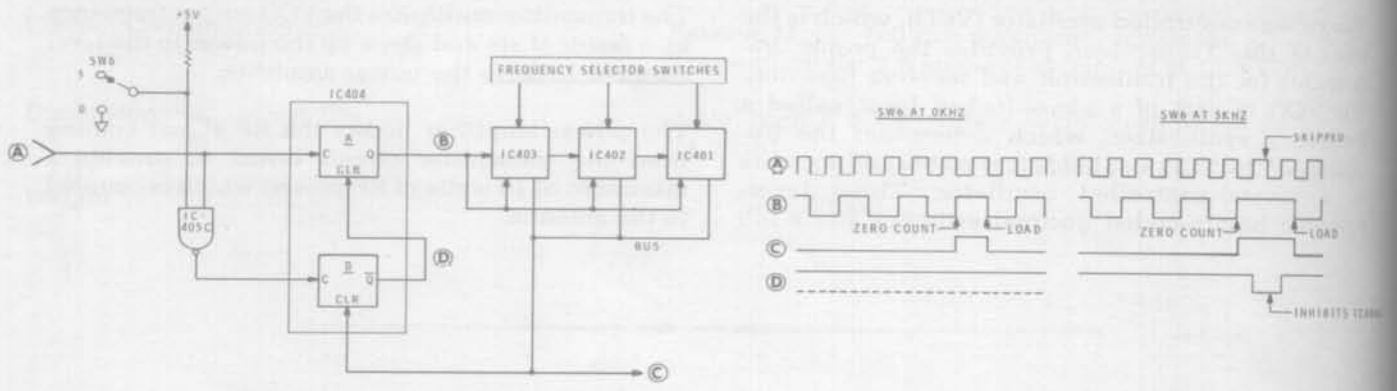


Figure 1

on the front panel switches, is "loaded" into the counters on the indicated negative edge, and each subsequent positive edge decrements this number by one. For example, if 6.94 (146.94 MHz) is selected, a 6 is loaded into IC401, a 9 into IC402, and a 4 into IC403. This makes the divisor 694. After 694 cycles have been counted, the "buss" line (common line between pins 12) goes high briefly. The resulting series of positive pulses on the bus line is the output of the programmable divider.

Flip-flop IC404A, just ahead of the cascaded counters, multiplies the total divisor by 2 which, in the example given, makes the total divisor 2 × 694 = 1388 (0/5 kHz switch is in the 0 kHz position). In the simplex (SIM) mode, the offset oscillator is operating at 23.333 MHz. If this is mixed with the required VCO frequency of 24.49 MHz (146.94 MHz/6), a difference frequency of 1.1567 MHz is obtained. If this difference is divided by 1388 (2 × 694), the result is 833.333 Hz, as required for lock.

If the 0/5 kHz switch is set to the 5 kHz position, the total divisor must increase by one to 1389 (2 × 694.5). This is accomplished by disabling IC404A during the cycle which just follows the positive edge of the buss output. In effect, IC404B counts the extra cycle and "hides" it from IC404A.

OFFSET OSCILLATOR

The offset oscillator is formed by Q406 and the associated circuitry. In the receive mode, the required oscillator frequency is 21.55 MHz. This crystal (Y405) is switched in by D406, which is turned on by Q412. Q412 conducts due to the 13.8 volts present on pin U via the relay coil.

In the transmit mode, the push-to-talk switch removes the base bias from Q413, which allows Q414 to turn on and energize the relay. Q411 and Q412 turn off and Q410 conducts, which switches in the appropriate transmitter offset crystal as selected by the front panel Mode switch, SW7.

OUT-OF-LOCK/BAND DETECTION AND TRANSMIT INHIBIT

Whenever the phase-locked loop is not locked, negative pulses will appear on one of the two inputs to IC405A. The active input is determined by whether the output of the programmable divider is higher or lower than the 833.333 Hz reference. Positive pulses at the output of IC405A charge capacitor C421, which turns on Q405. When Q405 is turned on, it applies a low to pin 4 of IC405B, which causes its output to go high and turn on Q409. Q409 prevents Q414 from turning on when you press the PTT switch and thus inhibits the transmitter. The low on pin 4 of IC405B is also applied to Q407, which turns it off and allows Q408 to light the Synth Lock LED.

If the 1 MHz lever switch (SW3) is set to a number other than 4, 5, 6, or 7, the "4" output of the switch is grounded. This grounds pin 5 of IC405B and inhibits the transmitter as was described in the above paragraph. This helps prevent you from operating outside the 2-meter amateur band. (Out-of-band transmissions can still occur when the selected receive frequency is within the band, but the offset transmitter frequency is not.) If MARS or CAP operation is desired, you can remove the jumper on the synthesizer circuit board to disable the out-of-band inhibit feature.

R448, R449, and C443 briefly delay the inhibit circuitry to allow the synthesizer to lock on different frequencies in transmit and receive. The delay gives the loop a chance to lock when the Transceiver switches from receive to transmit. This transition typically takes less than 150 mS, but if the loop does not re-lock within approximately 500 mS, the transmitter inhibit circuitry releases the relay.

IC502, an ECL (emitter-coupled logic) integrated circuit, is the heart of the VCO. It is tuned by L501, C513, and varactor diode VD502. In the receive mode, Q502 switches in C509 and C511 which lower the frequency range by the required amount. In transmit, frequency modulation is accomplished by applying the transmitter audio to a second varactor diode, VD501. This assures constant deviation over the entire frequency range.

Q503 and Q504 make up a low-pass filter, which helps remove any residual 833.333 Hz reference from the tune voltage.

IC501, a separate 5-volt regulator, is included on the VCO circuit board. This regulator supplies only the oscillator IC and loop filter and thus helps to isolate the analog circuitry from the digital circuitry.

SCHEMATIC OF THE
HEATHKIT®
SYNTHESIZED 2-METER FM TRANSCEIVER
MODEL HW-2036A

NOTES:

1. COMPONENT NUMBERS ARE IN THE FOLLOWING GROUPS.
   - 1-99 PARTS MOUNTED ON THE CHASSIS.
   - 100-199 PARTS MOUNTED ON THE TRANSMITTER CIRCUIT BOARD.
   - 200-299 PARTS MOUNTED ON THE RECEIVED CIRCUIT BOARD.
   - 300-399 PARTS MOUNTED ON THE SYNTHESIZER CIRCUIT BOARD.
   - 400-499 PARTS MOUNTED ON THE POWER AMPLIFIER CIRCUIT BOARD.
   - 500-599 PARTS MOUNTED ON THE VCO CIRCUIT BOARD.
2. ALL RESISTORS ARE 1/4-WATT, 5% TOLERANCE, UNLESS OTHERWISE NOTED. RESISTOR VALUES ARE IN OHMS: K=1000, M=1,000,000.
3. CAPACITORS LESS THAN 1 ARE IN µF (MICROFARADS), UNLESS OTHER CAPACITORS ARE IN pF (PICOFARADS), UNLESS OTHERWISE NOTED.
4. ARROWS AT CONTROLS INDICATE CLOCKWISE ROTATION AS VIEWED FROM THE SHAFT END OF THE CONTROL.
5. THIS SYMBOL INDICATES A POSITIVE DC VOLTAGE MEASURED WITH A HIGH IMPEDANCE VOLTMETER FROM THE POINT INDICATED TO CHASSIS GROUND UNDER THE FOLLOWING CONDITIONS:
   - RECEIVER SQUELCHED AT THRESHOLD.
   - VOLUME CONTROL FULLY COUNTERCLOCKWISE.
   - TRANSMITTER VOLTAGES KEYED WITHOUT MODULATION.
6. THIS SYMBOL INDICATES CIRCUIT BOARD GROUND.
7. THIS SYMBOL INDICATES CHASSIS GROUND.
8. THIS SYMBOL INDICATES A SOLDERED CONNECTION TO A CIRCUIT BOARD.
9. THIS SYMBOL INDICATES A COIL WOUND BY THE KIT BUILDER.
10. REFER TO THE "CIRCUIT BOARD X-RAY VIEWS" FOR THE PHYSICAL LOCATION OF PARTS.
11. THIS SYMBOL INDICATES A TEST POINT.
12. THIS VOLTAGE WAS MEASURED WITH A FULL QUIETING SIGNAL INPUT. MODULATED AT 1 kHz WITH ±3 kHz DEVIATION. AUDIO OUTPUT IS SET FOR 1 WATT INTO 8Ω IN AN 8Ω LOAD.
13. INPUT AT MICROPHONE.
14. MEASURED WITH NO SIGNAL INPUT.
15. ALL RECEIVER RF LEVELS WERE MEASURED WITH CIRCUIT IN FULL LIMITING.

Part of 595-2086-02